Hall Ticket Number:

Code No. : 22202

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. II Year (E.E.E.) II-Semester (Main) Examinations, May-2016

Digital Electronics and Logic Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Minimize the given Boolean expression using K-Map
   $F(A, B, C,D) = \Sigma m (0, 1, 2, 8, 9, 10, 11, 15)$.
2. List out the postulates of Boolean algebra.
3. Draw the basic NOR and NAND gate using RTL and DTL
4. Distinguish between encoder and decoder
5. Describe the operation of Full subtractor using truth table and draw its logic diagram.
6. Using 10's complement solve i) $(72532)_{10} - (3250)_{10}$ ii) $(45633)_{10} - (53244)_{10}$.
7. Design T-Flip-Flop using JK-Flip Flop
8. Is magnitude comparator a combinational or sequential circuit? Justify.
9. Differentiate between PLA and PAL.
10. Distinguish between synchronous and asynchronous counter.

Part-B (5 × 10 = 50 Marks)

11. a) Explain about incompletely specified function. Mention whether it is advantage or disadvantage. [4]
    b) Minimize the following Boolean function using K-Map [6]
    $F(A, B, C, D) = \prod M (1, 2, 3, 5, 7, 8, 10, 15)$.
12. a) Compare the performance of TTL, ECL and CMOS logic gates with reference to fan-in, fan-out, noise immunity and propagation delay. Give typical values in each case. [5]
    b) Design a combinational circuit using 2^{n-1}x1 Multiplexer to obtain the function [5]
    $F(n) = \Sigma m (0, 1, 4, 6, 8, 10, 13, 15)$
13. a) Design a BCD to Excess-3 Code converter. [5]
    b) Design a 4-bit Comparator. [5]
14. a) Give the truth table of JK Flip Flop and explain the principle of operation of clocked JK Flip Flop with output waveform. [5]
    b) Draw the logic diagram of a 3 bit up/down synchronous counter and explain its operation. [5]
15. a) Explain briefly about sequence detector. [4]
    b) Design a logic diagram for the given functions using PLA and PAL [6]
    $F_1 = \Sigma(0, 1, 2, 4, 5, 7)$ $F_2 = \Sigma(1, 5, 6, 7)$
16. a) Simplify the given function and implement with NAND gates. [2+2]
    $F(A, B, C, D) = AC' + ACE + A'CD' + ACE' + A'D'F'$
    $F(w, x, y, z) = (w' + x + y)(w + x' + y')$
    b) Design a 4 to 2 priority encoder and explain its operation in brief. [6]
17. Answer any ***two*** of the following:
    a) Advantage of Complement representation [5]
    b) Counters [5]
    c) State diagram for designing Counters [5]